WHAT IS CLAIMED IS:

1. A circuit for correcting bow in a linear arrangement of elements comprising:

a substrate assembly having a plurality of LED elements each having associated driver subassemblies, each of the LED elements representing a pixel within a line;

an interface board coupled to the substrate assembly, the interface board having circuitry that processes image data for the LED elements;

a course bow correction circuit on the interface board that electronically arranges the pixels to improve linearity by integral numbers of pixel pitch; and

a fine bow correction circuit located at least partially on the substrate, the fine bow correction circuit providing a first circuit common to a plurality of the LED elements and a second circuit dedicated to a specific LED element, the second circuit selecting one of a set of a delays that improves linearity of the pixels within the line by a fraction of a pixel pitch.

2. The circuit of claim 1 wherein the fine bow correction circuit is located entirely on the substrate.

3. The circuit of claim 1 wherein the fine bow correction circuit is located at least partially on the interface board.

4. The circuit of claim 3 wherein the fine bow correction circuit that is located at least partially on the interface board provides at least one circuit trace that carries a plurality of signals to the fine bow correction circuit on the substrate, wherein the signals are not concurrently active.

5. The circuit of claim 1 wherein the fine bow correction further comprises:

the first circuit providing the set of delays to the plurality of LED elements; and

the second circuit selecting one of the delays according to a specific parameter for the LED element.

6. The circuit of claim 5 wherein the parameter further comprises a stored value that selects one of delays.

7. The circuit of claim 6 wherein the stored value is within the fine bow correction circuit and further comprises at least one multiplexer and at least one latch per LED element.

8. The circuit of claim 1 further comprising a delay repeat circuit that creates multiples of the set of delays using the set of delays.

9. The printhead of claim 1 wherein the fine bow correction circuit is implemented at a segment level selected from one of the following groups: 2, 4, 8, or 16 LED elements.

10. The printhead of claim 1 wherein the interface board further comprises a set of printhead brightness tables and a set of printhead correction tables on the interface board.

11. The printhead of claim 1 wherein the LED elements are arranged in a plurality of rows and wherein the second circuit selects different delays for different rows.

12. The printhead of claim 11 wherein the plurality of rows further comprises an odd row and an even row, and the second circuit selects delays that are offset by one delay between the odd row and the even.

13. An electronic bow correction method comprising the steps of:

providing a linear arrangement of elements on a substrate having an ideal degree of linearity, each of the elements representing pixels having a predetermined pixel pitch and timing means for exposing the elements for a single line time period, the substrate being coupled to an interface board that provides image process electronics for the plurality elements on the substrate;

creating a first circuit that places the plurality elements within the single pixel pitch of the ideal degree of linearity;

forming a second circuit that comprises a plurality of delays which are each a fraction of the single pixel pitch and means for selecting one of the delays to be applied to the timing means in accordance with a predetermined parameter; and

placing the parameter within the means for selecting.

14. The method of bow correction within claim 13 wherein the means for selecting further comprises a register and a multiplexer configured to select one of the delays to the timing means in accordance with the predetermined parameter.

15. The method of claim 13 wherein the step of forming further comprises forming means for selecting having comprises a software accessible register.

16. The method of claim 15 wherein the step of forming further comprises forming the software accessible register such that it can be loaded via a JTAG serial data path.

17. The method of claim 13 wherein the step of forming further comprises forming the second circuit with a delay clock having a fixed clock reference for unique fixed delays which has a frequency that can be changed to produce different delay increments.

18. The method of claim 17 wherein the step of forming further comprises the second circuit having a delay repeat function that allows each of the delays to be used multiple times to increase the delays available within a line time.

19. The method of claim 13 wherein the step of forming the second circuit further comprises forming the second circuit such that it is located at least partially on the interface board and the part of the second circuit that is formed on the interface board provides at least one circuit trace that carries a plurality of signals to the second circuit portion located on the substrate, wherein the signals are not concurrently active.

20. The method of claim 13 wherein the providing step further comprises providing the elements arranged in a plurality of rows and wherein the predetermined parameter selects different delays for different rows.

21. The method of claim 20 wherein the plurality of rows further comprises an odd row and an even row, and the predetermined parameter selects delays that are offset by one delay between the odd row and the even row.

22. An electronic printing product having pixel alignment circuitry defined by the steps of:

providing a substrate having a plurality of printing elements with associated driver circuitry coupled to an interface

board, and timing means for selectively exposing each of the printing elements for a line time;

creating a coarse adjustment circuit on the interface board, the coarse adjustment circuit having circuitry that aligns pixel data in integral numbers of line times;

forming a fine adjustment circuit located at least partially on the substrate, the fine adjustment circuit providing a plurality of delays to each of the elements, wherein each of the delays is a fraction of an exposure period of the timing means; and

selecting one of the delays in accordance with a predetermined parameter.

23. The product of claim 22 circuit of claim 16 wherein the step of forming further comprises forming the fine adjustment circuit with a software accessible register for delay selection of each element.

24. The product of claim 22 wherein the step of forming further comprises forming the fine adjustment circuit wherein the software accessible register can be loaded via a JTAG serial data path.

25. The product of claim 24 wherein the step of forming further comprises forming the fine adjustment circuit wherein a delay clock having a fixed clock reference for unique fixed delays which has a frequency that can be changed to produce different delay increments.

26. The product of claim 22 wherein the step of forming further comprises forming the fine adjustment circuit wherein the plurality of delays are modifiable to allow for different levels of fine pixel adjustment.

27. The product of claim 22 wherein the step of forming the fine bow correction circuit forms the fine bow correction circuit such that it is located at least partially on the interface board and provides at least one circuit trace that carries a plurality of signals to the fine bow correction circuit on the substrate, wherein the signals are not concurrently active.

28. The product of claim 22 wherein the step of selecting further comprises selecting the delays such that the delays are repeated with a first delay following a last delay forming a repeated delay circuit from multiples of the delays.

29. The product of claim 22 wherein the step of providing further comprises providing the elements arranged in a plurality of rows and wherein the fine adjustment circuit selects different delays for different rows.

30. The product of claim 29 wherein the step of providing further comprises providing as the plurality of rows an odd row and an even row, and the fine adjustment circuit selects delays that are offset by one delay between the odd row and the even row.